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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,512	08/31/2001	Yasuo Osone	500.40530X00	8183

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/943,512	OSONE ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final..

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-23 and 25-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25, 27 46 and 47* is/are allowed.

6)☐ Claim(s) *14-23,26,28-45,48 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8-31-1, 2-17-4, 10-27-4, 4-10-6* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8-10-7 has been entered.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following claim features must be shown or the feature(s) canceled from the claim(s):

Re claim 14: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 15: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate

partly overlap areas which only the through holes in the multilayer wiring board occupy.

Re claim 16: an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is completely inside of a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 21: an in-plane distribution of heat dissipated from the transistor substantially coincides with distribution of the through holes.

Re claim 22: an in-plane distribution of heat dissipated from the transistor substantially coincides with in-plane distribution of large and small cross-section areas of the through holes.

Re claim 23: entire in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board

and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 26: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The specification is objected to as failing to provide proper antecedent basis for the following claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o):

Re claim 14: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 15: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which only the through holes in the multilayer wiring board occupy.

Re claim 16: an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is completely inside of a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 21: an in-plane distribution of heat dissipated from the transistor substantially coincides with distribution of the through holes.

Re claim 22: an in-plane distribution of heat dissipated from the transistor substantially coincides with in-plane distribution of large and small cross-section areas of the through holes.

Re claim 23: entire in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 26: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter is the following:

Re claim 14: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate

are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 15: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which only the through holes in the multilayer wiring board occupy.

Re claim 16: an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is completely inside of a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 23: entire in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board

and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Red 26: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

To further clarify, there is no basis in the original disclosure for the negative limitation "only the through holes in the multilayer wiring board occupy."

Any negative limitation or exclusionary proviso must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation or drawing illustration is not basis for an exclusion.

Claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The undescribed subject matter is the following:

Re claim 14: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 15: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which only the through holes in the multilayer wiring board occupy.

Re claim 16: an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is completely inside of a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate

are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 23: entire in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Red 26: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

To further clarify, one skilled in the art would be unable to make and/or use the invention because the language, "areas which only the through holes in the multilayer wiring board occupy" excludes the inclusion of additional elements such as the semiconductor substrate through holes and heat dissipating regions.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 14-23, 26, 28-45, 48 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of the following language is unclear:

Re claim 14: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 15: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which only the through holes in the multilayer wiring board occupy.

Re claim 16: an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is completely inside of a through hole or an area where only through holes are built in the multilayer wiring board.

Re claim 17: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Re claim 23: entire in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

Red 26: entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas which only the through holes in the multilayer wiring board occupy.

To further clarify, the language, "areas which only the through holes in the multilayer wiring board occupy" appears to preclude the inclusion of the semiconductor substrate through holes and heat dissipating regions in the areas.

The following is a quotation of MPEP 2111.01 [R-3] Plain Meaning:

I. THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION

While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, **>367 F.3d 1359, 1369, 70 USPQ2d 1827, 1834 (Fed. Cir. 2004)< (The USPTO uses a different standard for construing claims than that used by district courts; during examination the USPTO must give claims their broadest reasonable interpretation.). This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004) (Ordinary, simple English words whose meaning is clear and unquestionable, absent any indication that their use in a particular context changes their meaning, are construed to mean exactly what they say. Thus, "heating the resulting batter-coated dough to a temperature in the range of about 400oF to 850oF" required heating the dough, rather than the air inside an oven, to the specified temperature.). One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification. See, e.g., Liebel-Flarsheim Co. v. Medrad Inc., 358 F.3d 898, 906, 69 USPQ2d 1801, 1807 (Fed. Cir. 2004)(discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment). It is only when the specification provides definitions for terms appearing in the claims that the specification can be used in interpreting claim language. In re Vogel, 422 F.2d 438, 441, 164 USPQ 619, 622 (CCPA 1970). See also Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875, 69 USPQ2d 1865, 1868 (Fed. Cir. 2004) ("Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment."); E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) ("Interpretation of descriptive statements in a patent's written description is a difficult task, as an inherent tension exists as to whether a statement is a clear lexicographic definition or a description of a preferred embodiment. The problem is to interpret claims in view of the specification' without unnecessarily importing limitations from the specification into the claims."); Altiris Inc. v. Symantec Corp., 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003) (Although the specification discussed only a single embodiment, the court held that it was improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order on the performance of the method steps, and the specification did not directly or implicitly require a particular order). See also paragraph III., below. There is one exception, and that is when an element is claimed using language falling under the scope of 35 U.S.C. 112, 6th paragraph (often broadly referred to as means or step plus function language). In that case, the specification must be consulted to determine the structure, material, or acts corresponding to the function recited in the claim. In re Donaldson, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994) (see MPEP § 2181- §

2186). In In re Zletz, supra, the examiner and the Board had interpreted claims reading "normally solid polypropylene" and "normally solid polypropylene having a crystalline polypropylene content" as being limited to "normally solid linear high homopolymers of propylene which have a crystalline polypropylene content." The court ruled that limitations, not present in the claims, were improperly imported from the specification. See also In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) ("Claims are not to be read in a vacuum, and limitations therein are to be interpreted in light of the specification in giving them their broadest reasonable interpretation'." 710 F.2d at 802, 218 USPQ at 292 (quoting In re Okuzawa, 537 F.2d 545, 548, 190 USPQ 464, 466 (CCPA 1976)) (emphasis in original). The court looked to the specification to construe "essentially free of alkali metal" as including unavoidable levels of impurities but no more.). Compare In re Weiss, 989 F.2d 1202, 26 USPQ2d 1885 (Fed. Cir. 1993) (unpublished decision - cannot be cited as precedent) (The claim related to an athletic shoe with cleats that "break away at a preselected level of force" and thus prevent injury to the wearer. The examiner rejected the claims over prior art teaching athletic shoes with cleats not intended to break off and rationalized that the cleats would break away given a high enough force. The court reversed the rejection stating that when interpreting a claim term which is ambiguous, such as "a preselected level of force", we must look to the specification for the meaning ascribed to that term by the inventor." The specification had defined "preselected level of force" as that level of force at which the breaking away will prevent injury to the wearer during athletic exertion. It should be noted that the limitation was part of a means plus function element.)

In claims 21 and 22 the scope of the language "in-plane distribution" is unclear because the language is not clearly defined in the disclosure, and it otherwise has no plain meaning.

Claims 14-23, 26, 28-45, 48 and 49 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions

that must be made as to the scope of the claims. Also see In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06.

Applicant's amendment and remarks filed 8-20-7 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant asserts, "as clearly shown in Figs. 2 and 5 (and discussed, for example, on page 19, line 5 et seq. of the original specification), the entire area occupied by the via holes 5 is included only within the area occupied by the thermal vias 4 in the XY plane in the Figs.."

This assertion is respectfully deemed unpersuasive because the scope of the claims is not so limited.

Applicant also contends, "each of the rejected independent claims have been amended to clarify that the entire areas of the through holes of the semiconductor substrate are included "in areas which only the through holes in the multilayer wiring board occupy." It is respectfully submitted that this serves to clearly define the arrangement, such as shown in Fig. 2(c) while clearly distinguishing over the arrangement shown in the Prior Art Fig. 4.

This contention is respectfully traversed because Fig. 2(c) does not show areas which only the through holes in the multilayer wiring board occupy. For example, Fig. 2(c) shows areas in which the through holes in the multilayer wiring board and the emitter electrodes 7 occupy.

Claims 25, 27 46 and 47 are allowed.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.

19-Oct-07